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(71) Applicant: TDK CORP

(72) Inventor: FUJISHIRO YOSHIKAZU
TOGASHI MASAAKI

(54) CAPACITOR ARRAY

(57) Abstract:

PURPOSE: To provide a capacitor array capable of reducing crosstalk, regarding a capacitor array wherein a plurality of individual inner electrodes and common inner electrodes are formed inside dielectrics via a dielectric layer.

CONSTITUTION: Individual inner electrodes 2a-2f are divided into groups for a plurality of electrodes. Common inner electrodes 3a, 3b which inclusively face the whole group are divided and arranged in each of the groups. The divided and arranged common inner electrodes 3a, 3b are connected, on outer electrodes 5a, 5b of dielectric side surfaces.

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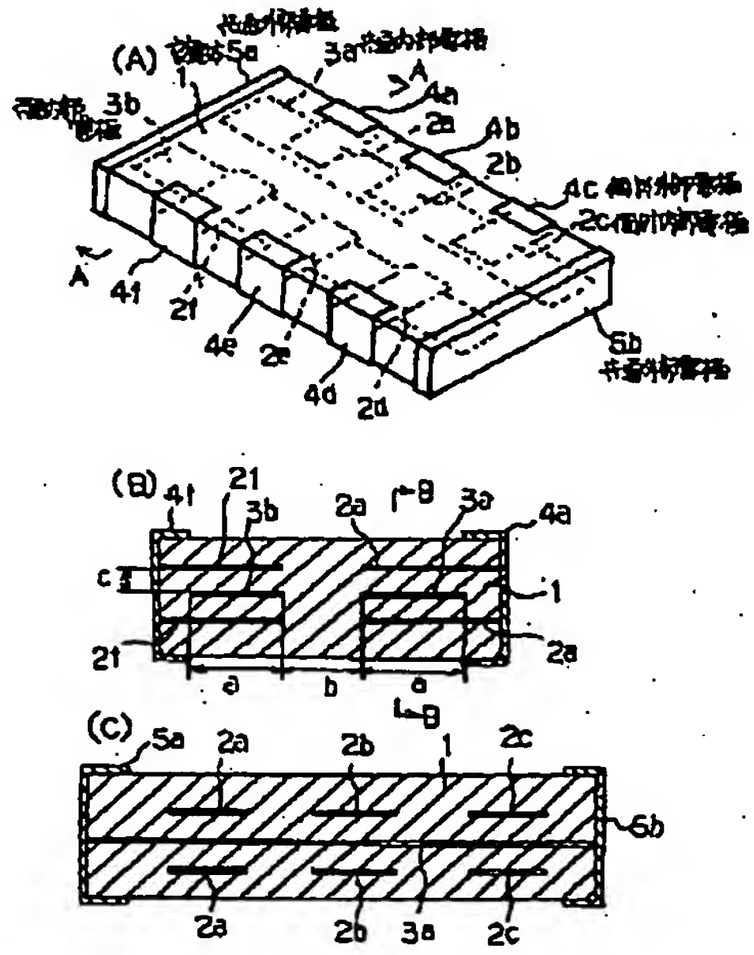

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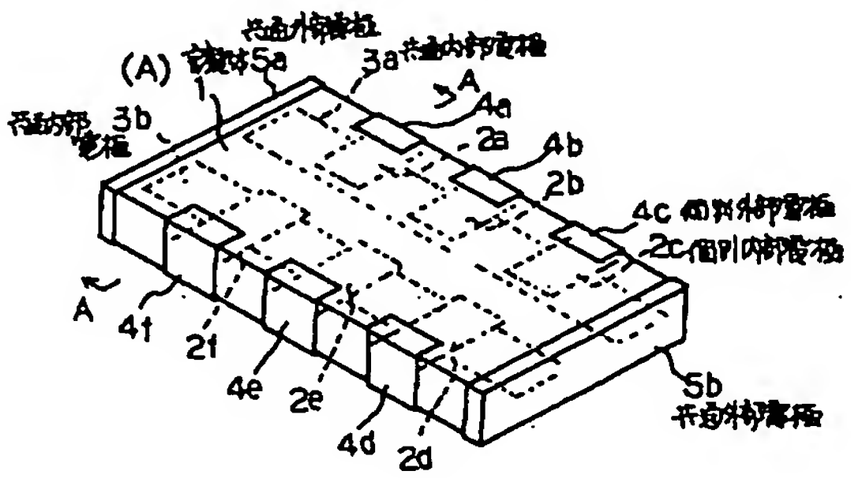
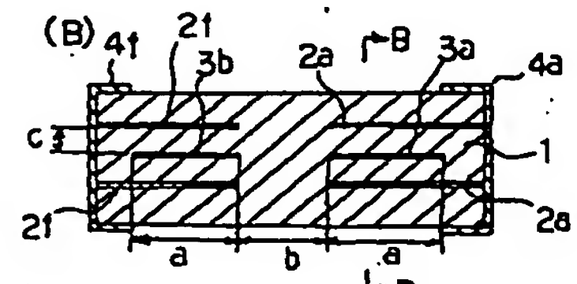
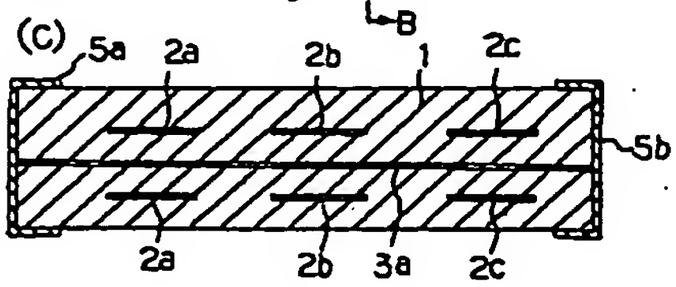
(71)出願人　000003067
ティーディーケイ株式会社
東京都中央区日本橋1丁目13番1号
(72)発明者　藤城　義和
東京都中央区日本橋一丁目13番1号　ティーディーケイ株式会社内
(72)発明者　富樫　正明
東京都中央区日本橋一丁目13番1号　ティーディーケイ株式会社内
(74)代理人　弁理士　若田　勝一

(54)【発明の名称】　コンデンサアレイ

(57)【要約】
【目的】誘電体の内部に、複数の個別内部電極と、共通内部電極とを誘電体層を介して形成したコンデンサアレイにおいて、クロストークを低下させることができるものを提供する。
【構成】個別内部電極２ａ～２ｆを複数の電極毎にグループ分けし、各グループ毎に、グループ全体に対して総括的に対向する共通内部電極３ａ、３ｂを分割配置すると共に、分割配置した共通内部電極３ａ、３ｂを誘電体側面の外部電極５ａ、５ｂにおいて接続した。







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【特許請求の範囲】

【請求項１】誘電体の内部に、複数の個別内部電極と、共通内部電極とを誘電体層を介して形成したコンデンサアレイにおいて、前記個別内部電極を複数の電極毎にグループ分けし、各グループ毎に、グループ全体に対して総括的に対向する共通内部電極を分割配置すると共に、分割配置した共通内部電極を誘電体側面の外部電極において接続したことを特徴とするコンデンサアレイ。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、シート法や印刷法等の成膜法によって積層して構成され、誘電体内に、複数の個別内部電極と、これらに共通に誘電体層を介して対向する共通内部電極とを形成して複数のコンデンサを内蔵したコンデンサアレイに関する。

【０００２】

【従来の技術】コンデンサアレイは、１個のチップに多数のコンデンサを内蔵しているので、多数のコンデンサを必要とする場合に、１個のチップで済み、実装コストや基板専有面積の面で有利である。このようなコンデンサアレイとして、実開平１－７９８１７号公報に開示されているように、誘電体内に櫛歯のように配列した個別内部電極に対し、櫛歯状に形成した内部電極をそれぞれ個別に対面させ、これらの共通内部電極を共通の内部導体パターンを介して誘電体側面に引き出して外部電極に接続したものがある。

【０００３】また、図４（Ａ）は本発明者等が開発した従来のコンデンサアレイの斜視図であり、図４（Ｂ）は（Ａ）のＥ－Ｅ断面図、（Ｃ）は（Ｂ）のＦ－Ｆ断面図、（Ｄ）は等価回路図である。このコンデンサアレイは、誘電体１内に形成した個別内部電極２ａ～２ｆに対して前記櫛歯状ではなく、個別内部電極２ａ～２ｆの全体に総括的に対向するような矩形板状の共通内部電極３を形成し、個別内部電極２ａ～２ｆは誘電体１の対向する２つの側面の個別外部電極４ａ～４ｆに接続し、共通内部電極３は、対向する他の対向する２側面の共通外部電極５ａ、５ｂに接続してなる。

【０００４】図５は図４に示したコンデンサアレイのシート法による製造工程を１個のチップ分について示す図であり、図５（Ａ）に示すように、誘電体シート１ａを必要枚数積層し、次に図５（Ｂ）に示すように、誘電体シート１ｂ上に個別内部電極２ａ～２ｆを印刷等により形成したものを重ね、その上に図５（Ｃ）に示すように、誘電体シート１ｃ上に共通内部電極３を形成したものを重ね、その後、前記個別内部電極２ａ～２ｆを形成した誘電体シート１ｄを重ね（図５（Ｄ））、さらにその上に必要枚数の誘電体シート１ｅを重ね、加圧、切断、焼成等の工程を経、その後に前記外部電極４ａ～４ｆ、５ａ、５ｂを焼き付けやメッキ等によって形成する。このよう構成されたコンデンサ回路は図4（Ｄ）に

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示すように表される。

【０００５】

【発明が解決しようとする課題】しかし、前記実開平１－７９８１７号公報に開示されたコンデンサアレイのように、櫛歯状の共通内部電極が内部導体パターンを介して共通外部電極に接続されたものにおいては、前記共通内部電極の内部導体パターンに個別電極の電流が共通に流れ、その内部導体パターンの線幅が狭くなりため、その内部導体パターンにおける損失の増大により、Ｑが低下すると共に、クロストーク（１個の素子に信号が来た時に信号の来ていない別の素子にその一部が漏れて伝わる現象）が発生するというという問題点がある。また、このようなＱの低下を防止するためには、前記内部導体パターンを分厚く形成する必要があり、チップの大形化を招く。

【０００６】一方、図４に示したコンデンサアレイは、共通内部電極３が全個別内部電極２ａ～２ｆ全体に総括的に対向する広さに形成されているので、共通内部電極３の流路断面積が広くなり、前記Ｑの低下の問題は緩和され、薄形化が達成できるものの、やはりクロストークの発生があり、特に数１０MHz以上の高周波におけるクロストークが顕著になる。このようなクロストークは、信号が漏れて来た側には不必要が信号であり、雑音である。このような雑音は機器の誤動作を招く。

【０００７】本発明は、上記した問題点に鑑み、クロストークを低下させることができるコンデンサアレイを提供することを目的とする。

【０００８】

【課題を解決するための手段】本発明は、上記目的を達成するため、誘電体の内部に、複数の個別内部電極と、共通内部電極とを誘電体層を介して形成したコンデンサアレイにおいて、前記個別内部電極を複数の電極毎にグループ分けし、各グループ毎に、グループ全体に対して総括的に対向する共通内部電極を分割配置すると共に、分割配置した共通内部電極を誘電体側面の外部電極において接続したことを特徴とする。

【０００９】

【作用】本発明においては、複数の個別内部電極からなるグループに対して総括的に対向する共通内部電極を設けることにより、共通内部電極の電流の断面積を確保でき、共通内部電極における損失の増大を防止できる。また、グループ毎に共通内部電極を分割したので、異なるグループ間の個別内部電極間のクロストークは減少する。

【００１０】

【実施例】図１（Ａ）は本発明によるコンデンサアレイの一実施例を示す斜視図、図１（Ｂ）は（Ａ）のＡ－Ａ断面図、（Ｃ）は（Ｂ）のＢ－Ｂ断面図である。本実施例が前記従来例と異なる点は、個別内部電極を、矩形をなすコンデンサアレイの片側（長辺）の側面に配列され

た個別外部電極４ａ～４ｃにそれぞれ接続される個別内部電極２ａ～２ｃのグループと、個別外部電極４ａ～４ｃの反対側の側面（長辺）に設けた個別外部電極４ｄ～４ｆにそれぞれ接続される個別内部電極２ｄ～２ｆからなるグループに分け、これらの各グループにそれぞれ総括的に対向するように（すなわち櫛歯状にして個別に対向するのではない）、共通内部電極を帯状に形成した２本の電極３ａ、３ｂに分割する。そして、これらの共通内部電極３ａ、３ｂの両端を共通に、アレイの短辺の共通外部電極５ａ、５ｂを接続する。

【００１１】図２は図５に対応して描いた製造工程を示す図であり、図２（Ｃ）の共通内部電極３ａ、３ｂを誘電体シート１ｃ上に形成している点が図５の従来例と異なっている。

【００１２】図３は本実施例と従来例のクロストークを比較して示す図であり、このクロストークを測定した実施例のコンデンサアレイは、電極にPdを用い、誘電体にチタン酸バリウム系を用い、縦横の寸法が６．３㎜×３．２㎜、厚さが１．０㎜のコンデンサアレイにおいて、図１（Ｂ）に示す共通内部電極３ａ、３ｂの幅ａを１．２㎜、共通内部電極３ａ、３ｂ間の間隔ｂを０．２㎜、個別内部電極２ａ～２ｆと共通内部電極３ａ、３ｂとの間隔ｃを１０μｍとした。一方図４の従来例におけるコンデンサアレイは、共通内部電極３の幅ｄを２．６㎜とし、他は本実施例と同じとした。図３はいずれも隣接する個別内部電極２ａと２ｆ間のクロストークを周波数に対応させて描いており、従来例においては、１００MHzで約－４０dBのクロストークがあったのに対し、本実施例においては、約－５５dBとなり、－１５dB程クロストークが減少した。なお、本実施例における個別内部電極２ａ－２ｂ間、すなわち同じグループ間のクロストークは従来例と同じであった。

【００１３】このように、複数の個別内部電極からなるグループをカバーしうるように、総括的に対向するように共通内部電極３ａ、３ｂを設けたので、異なるグループ間のクロストークが減少する上、櫛歯状の複数の共通内部電極に対して内部導体パターンを介して外部電極に

接続する従来例に比較して、損失を低減できる。また、共通内部電極３ａ、３ｂの無い部分は上下の誘電体により結合されているので、結合が強まり、誘電体シート間が剥離しにくくなり、強度の大きなチップが提供できるという効果もある。

【００１４】本発明において、個別内部電極２ａ～２ｆの同層における数や層数は目的に応じて種々に選択される。

【００１５】

【発明の効果】本発明によれば、複数の共通内部電極をグループ分けして各グループ毎に共通内部電極を分割したので、各グループ間について信号が伝播しにくくなり、グループ間のクロストークを減少させることができ、全体的に見て、クロストークを減少させることができる。また、共通内部電極は、グループ対応に総合的に対向するように設けられているので、流路断面積が確保され、損失を減少させ、個別内部電極対向に櫛歯状に形成する従来例に比較して、Ｑ値を向上させることができる。また、共通内部電極を分割しない構造に比較し、グループ対応の共通内部電極間が誘電体によって結合されるので、強度の大きなチップが提供できる。

【図面の簡単な説明】

【図１】（Ａ）は本発明によるコンデンサアレイの一実施例を示す斜視図、（Ｂ）はそのＡ－Ａ断面図、（Ｃ）は（Ｂ）のＢ－Ｂ断面図である。

【図２】本実施例の製造工程の一例を示す図である。

【図３】本実施例と従来例のクロストーク特性を比較して示す図である。

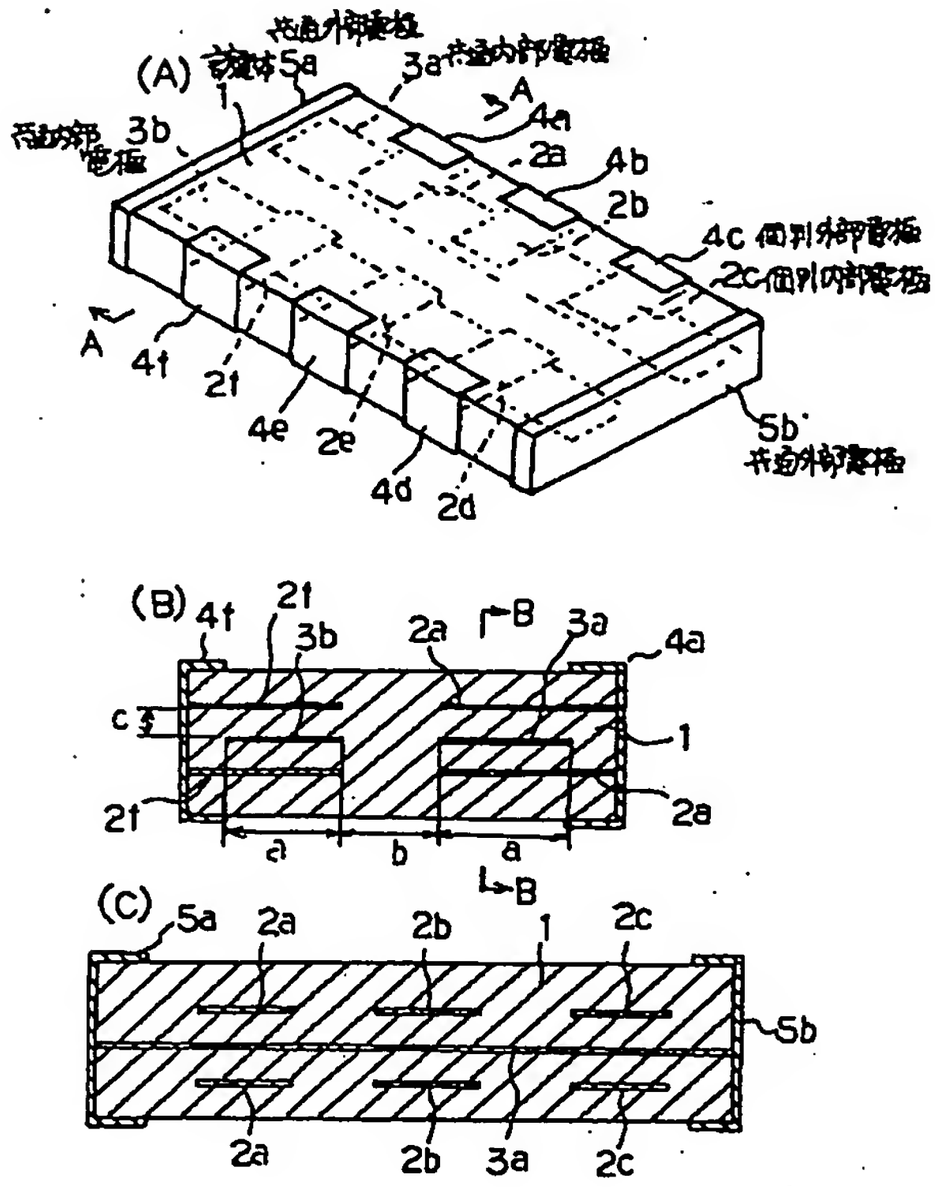
【図４】（Ａ）は従来のコンデンサアレイを示す斜視図、（Ｂ）はそのＥ－Ｅ断面図、（Ｃ）は（Ｂ）のＦ－Ｆ断面図、（Ｄ）は等価回路図である。

【図５】従来例の製造工程を示す図である。

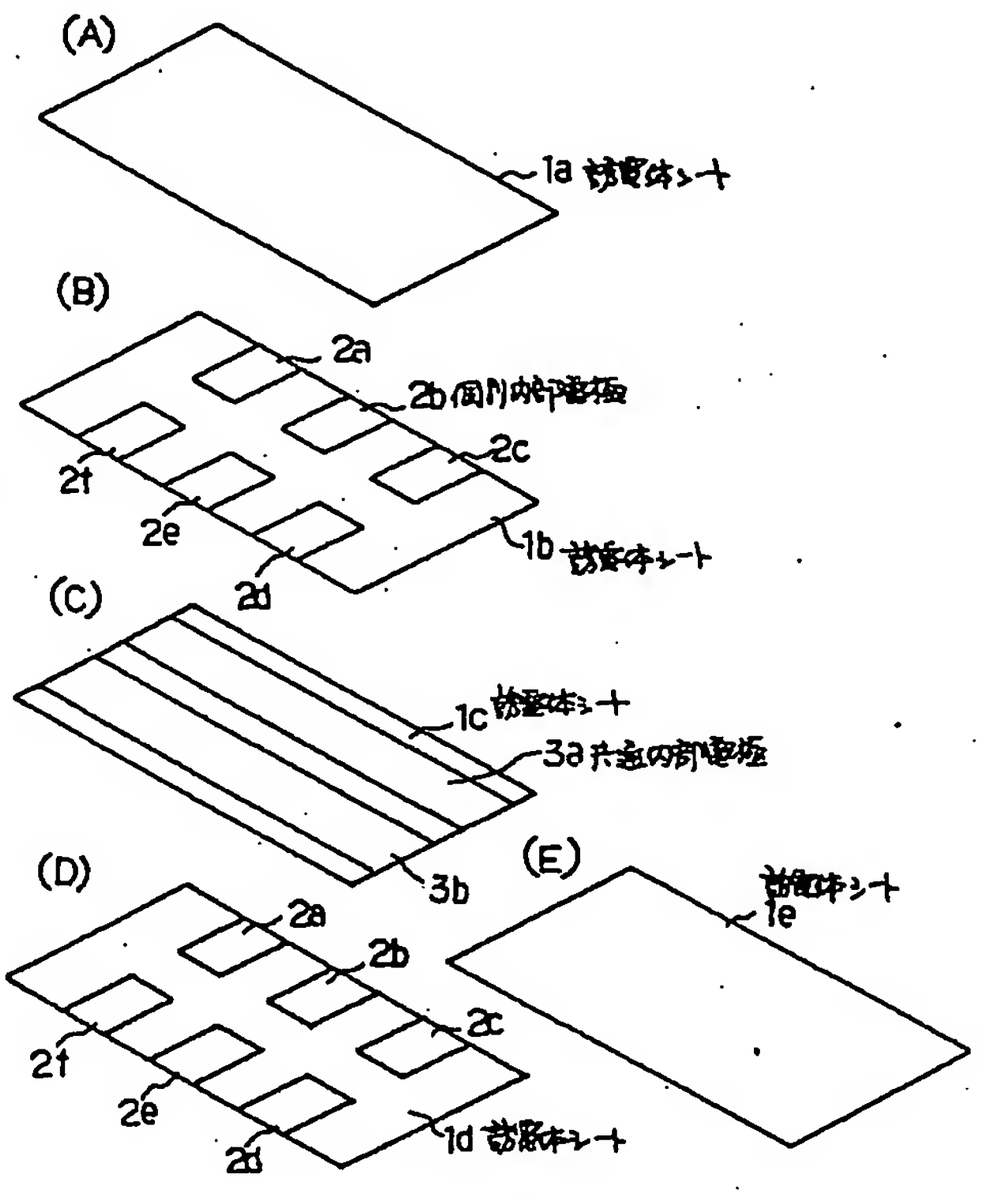
【符号の説明】

１：誘電体、２ａ～２ｆ：個別内部電極、３ａ、３ｂ：共通内部電極、４ａ～４ｆ：個別外部電極、５ａ、５ｂ：共通外部電極

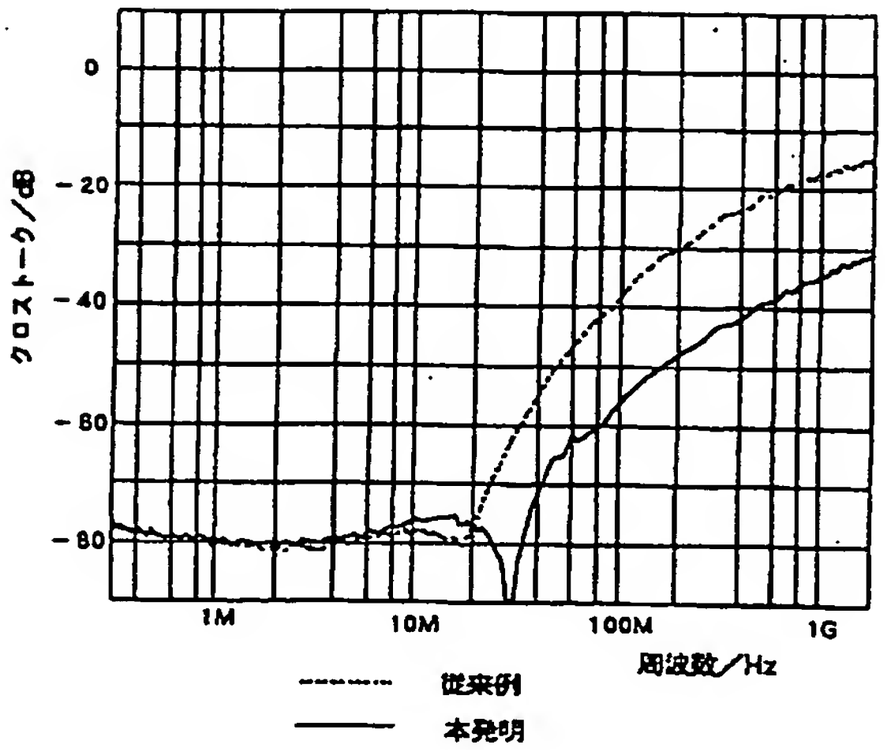
【図1】


(A)
5a
3a
4a
3b
2a
4b
2b
4c
2c
A
4f
2f
4e
2e
4d
2d
5b
(B)
4f
2f
3b
2a
3a
4a
B
c
1
a
b
a
(C)
5a
2a
2b
1
2c
5b

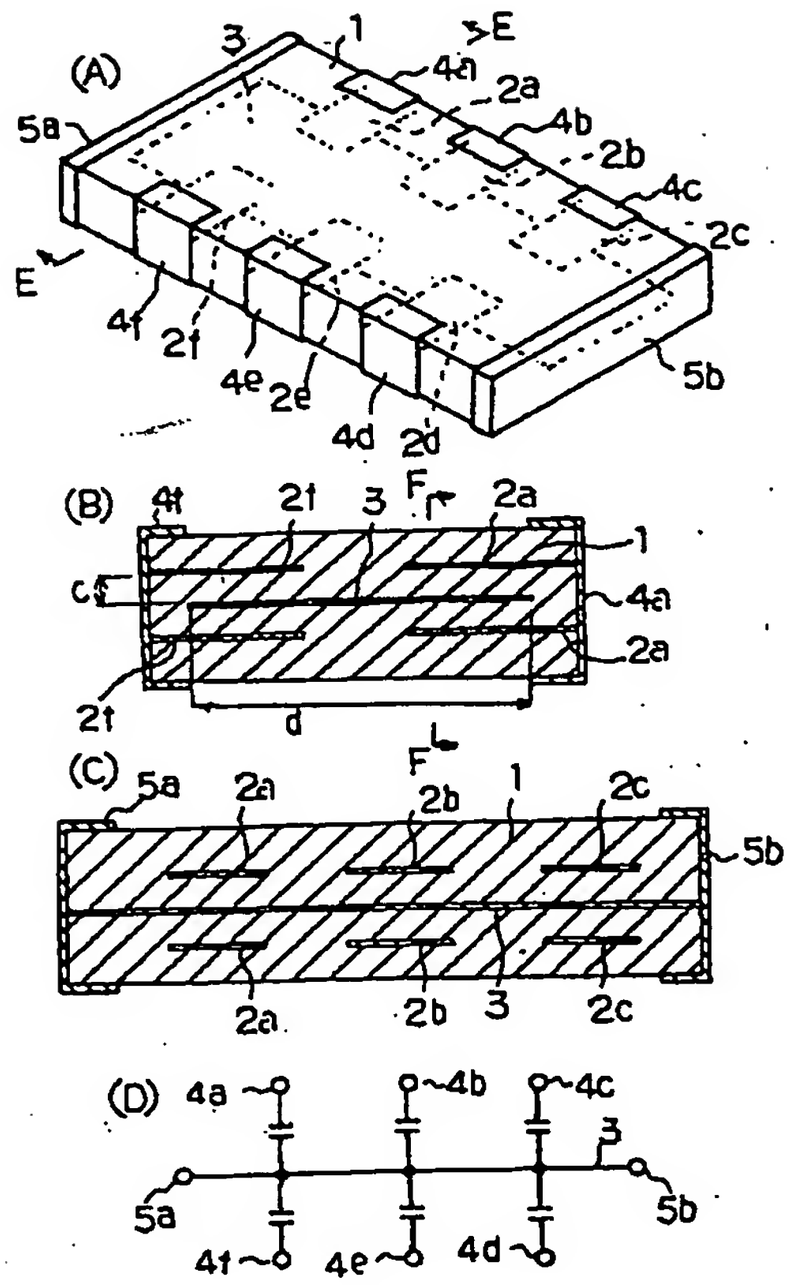
【図2】


(A)
1a
(B)
2a
2b
2c
2f
2e
2d
1b
(C)
1c
3a
3b
(D)
2a
2b
2c
2f
2e
2d
1d
(E)
1e

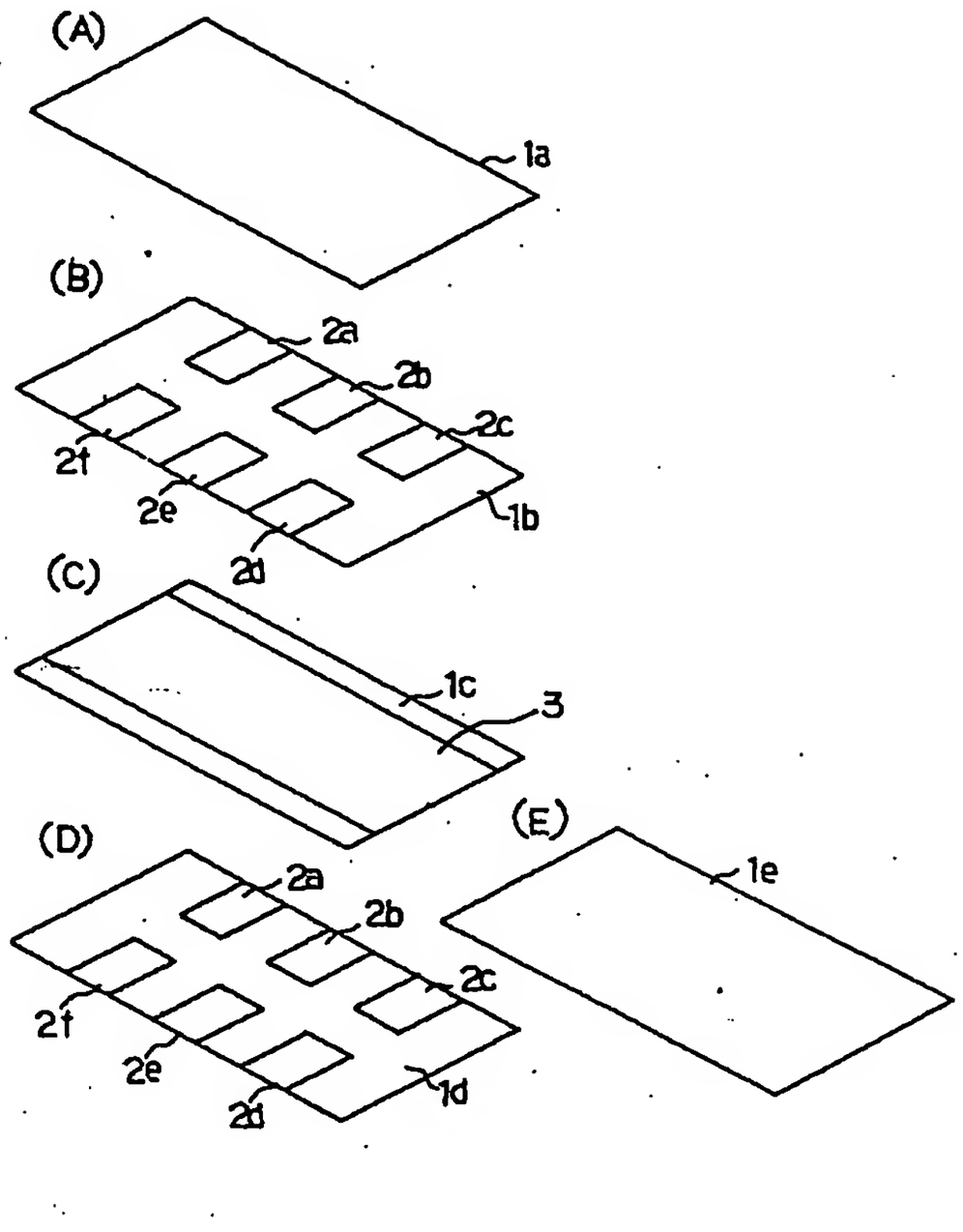
【図3】


0
−20
−40
−60
−80
クロストーク/dB
1M
10M
100M
1G
周波数/Hz
従来例
本発明

【図4】


(A)
3
1
E
4a
2a
4b
2b
4c
2c
5a
E
4f
2f
4e
2e
4d
2d
5b
(B)
4f
2f
3
F
2a
1
4a
2a
2f
d
(C)
5a
2a
2b
1
2c
5b
2a
2b
3
2c
(D)
4a
4b
4c
3
5a
5b
4f
4e
4d

【図5】


(A)
1a
(B)
2a
2b
2c
2f
2e
2d
1b
(C)
1c
3
(D)
2a
2b
2c
2f
2e
2d
1d
(E)
1e

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PURPOSE: To provide a capacitor array capable of reducing crosstalk, regarding a capacitor array wherein a plurality of individual inner electrodes and common inner electrodes are formed inside dielectrics via a dielectric layer.
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CLAIMS

[Claim(s)]
[Claim 1]The capacitor array characterized by connecting the common internal electrode which carried out division arrangement in the external electrode of a dielectric side face while carrying out division arrangement of the common internal electrode which counters said individual internal electrode in the gross to the whole group for every group part opium poppy and group for two or more electrodes of every in the capacitor array which formed two or more individual internal electrodes and a common internal electrode in the interior of a dielectric through the dielectric layer.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]By the forming-membranes methods, such as the sheet method and print processes, the laminating of this invention is carried out, it is constituted, and relates to the capacitor array which formed two or more individual internal electrodes and the common internal electrode which counters through a dielectric layer common to these, and built in two or more capacitors in the dielectric.
[0002]
[Description of the Prior Art]Since it builds many capacitors in one chip, when it needs many capacitors, a capacitor array can be managed with one chip and is advantageous in respect of mounting cost or substrate monopoly area. As such a capacitor array, there are some which the internal electrode formed in the shape of a ctenidium to the individual internal electrode arranged like a ctenidium in the dielectric was made to meet according to an individual, respectively, pulled out these common internal electrodes on the dielectric side face through the common inner conductor pattern, and were connected to the external electrode as indicated by JP,1-79817,U.
[0003]Moreover, drawing 4 (A) is the perspective view of the conventional capacitor array which this invention person etc. developed, and drawing 4 (B) is [the F-F sectional view of (B) and (D of the E-E sectional view of (A) and (C))] representative circuit schematics. This capacitor array does not have the shape of said ctenidium to the individual internal electrodes 2a-2f formed in the dielectric 1. The rectangle tabular common internal electrode 3 which counters the individual internal electrodes [2a-2f] whole in the gross is formed. It connects with the individual external electrodes 4a-4f of two side faces in which a dielectric 1 counters, and the individual internal electrodes 2a-2f come to connect the common internal electrode 3 with the community external electrodes 5a and 5b of two side faces in which the others which counter counter.
[0004]As it is drawing showing one chip and the production process by the sheet method of a capacitor array shown in drawing 4 is shown in drawing 5 (A), drawing 5As the need number-of-sheets laminating of the dielectric sheet 1a is carried out and it is shown in drawing 5 (B) belowAs what formed the individual internal electrodes 2a-2f by printing etc. on dielectric sheet 1b is piled up and it is shown on it at drawing 5 (C)The thing in which the common internal electrode 3 was formed on dielectric sheet 1c is piled up. After that, Dielectric sheet 1d in which said individual internal electrodes 2a-2f were formed is piled up (drawing 5 (D)), dielectric sheet 1e of need number of sheets is further piled up on it, it passes through processes, such as pressurization, cutting, and baking, and said external electrodes 4a-4f, and 5a and 5b are formed by baking, plating, etc. after that. The capacitor circuit by which the such configuration was carried out

is expressed as shown in drawing 4 (D).
[0005]
[Problem(s) to be Solved by the Invention]However, it sets like the capacitor array indicated by said JP,1-79817,U to that by which the common ctenidium-like internal electrode was connected to the community external electrode through the inner conductor pattern. The current of an individual electrode flows in common to the inner conductor pattern of said common internal electrode, the line breadth of the inner conductor pattern becomes narrow, and accumulate, and according to increase of the loss in the inner conductor pattern, while Q fallsThere is a trouble of it being said that a cross talk (phenomenon in which the part leaks and gets across to another component by which a signal is not coming when a signal comes to one component) occurs. Moreover, in order to prevent the fall of such Q, it is necessary to form said inner conductor pattern thick, and large-sized-ization of a chip is caused.
[0006]On the other hand, since the capacitor array shown in drawing 4 is formed in the size which counters in the gross [the common internal electrode 3] to full-individual internal electrode 2a-2f of the whole, although the passage cross section of the common internal electrode 3 becomes large, and, as for the problem of a fall of said Q, is eased and thin form-ization can be attained, there is generating of a cross talk too and the cross talk in RF several 10MHz or more becomes remarkable especially. The non-need is a signal at the side from which the signal has leaked, and such a cross talk is a noise. Such a noise causes malfunction of a device.
[0007]This invention aims at offering the capacitor array to which a cross talk can be reduced in view of the above-mentioned trouble.
[0008]
[Means for Solving the Problem]In the capacitor array which formed two or more individual internal electrodes and a common internal electrode in the interior of a dielectric through the dielectric layer in order that this invention might attain the above-mentioned purposeWhile carrying out division arrangement of the common internal electrode which counters said individual internal electrode in the gross to the whole group for every group part opium poppy and group for two or more electrodes of every, it is characterized by connecting the common internal electrode which carried out division arrangement in the external electrode of a dielectric side face.
[0009]
[Function]In this invention, by preparing the common internal electrode which counters in the gross to the group who consists of two or more individual internal electrodes, the cross section of the current of a common internal electrode can be secured, and increase of the loss in a common internal electrode can be prevented. Moreover, since the common internal electrode was divided for every group, the interior [of individual] inter-electrode cross talk between different groups decreases.
[0010]
[Example]The A-A sectional view of (A) and (C of the perspective view and drawing 1 (B) which show one example of the capacitor array according [drawing 1 (A)] to this invention) are the B-B sectional views of (B). With the group of the individual internal electrodes 2a-2c connected to the individual external electrodes 4a-4c with which the point that this example differed from said conventional example was arranged in the individual internal electrode on the side face of one side (long side) of the capacitor array which makes a rectangle, respectivelyIt divides into the group who consists of individual internal electrodes 2d-2f connected to the individual external electrodes 4d-4f prepared in the side face (long side) of the opposite side of the individual external electrodes 4a-4c, respectively. A common internal electrode is divided into two electrodes 3a and 3b formed in band-like so that each of these groups may be countered in the gross, respectively (that is, it is made the shape of a ctenidium and does not counter according to an individual). And the community external electrodes 5a and 5b of the shorter side of an array are connected for

the both ends of these common internal electrodes 3a and 3b in common.

[0011]Drawing 2 is drawing showing the production process drawn corresponding to drawing 5, and the point which forms the common internal electrodes 3a and 3b of drawing 2 (C) on dielectric sheet 1c differs from the conventional example of drawing 5.
[0012]Drawing 3 is drawing comparing and showing the cross talk of this example and the conventional example, and the capacitor array of the example which measured this cross talkIn the capacitor array whose dimension in every direction is 6.3mmx3.2mm and whose thickness Pd is used for an electrode, a barium titanate system is used for a dielectric, and is 1.0mmSpacing c of 0.2mm, the individual internal electrodes 2a-2f, and the common internal electrodes 3a and 3b was set [the width of face a of the common internal electrodes 3a and 3b shown in drawing 1 (B)] to 10 micrometers for the spacing b between 1.2mm, common internal electrode 3a, and 3b. On the other hand, the capacitor array in the conventional example of drawing 4 set width of face d of the common internal electrode 3 to 2.6mm, and others made it the same as this example. The cross talk for adjoining individual internal electrode 2a and 2f is made to correspond to a frequency, and is drawn, it sets for the conventional example, and each drawing 3 is [about] at 100MHz. -To there having been a 40dB cross talk, it sets to this example and is [about]. -It was set to 55dB and the cross talk decreased by about -15dB. In addition, the cross talk between individual internal electrode 2a-2bs in this example (i.e., between the same groups) was the same as the conventional example.

[0013]Thus, since the common internal electrodes 3a and 3b were formed so that the group who consists of two or more individual internal electrodes could be covered, and it might counter in the gross, when the cross talk between different groups decreases, loss can be reduced as compared with the conventional example connected to an external electrode through an inner conductor pattern to two or more common ctenidium-like internal electrodes. Moreover, since it is combined with the up-and-down dielectric, association becomes strong, between dielectric sheets stops being able to exfoliate easily and the part without the common internal electrodes 3a and 3b is effective in the ability to offer a strong big chip.
[0014]in this invention, individual internal electrodes [2a-2f] the number and number of layers in this layer are chosen as versatility according to the purpose.
[0015]
[Effect of the Invention]Since according to this invention the group division of two or more common internal electrodes was carried out and the common internal electrode was divided for every group, it is hard coming to spread a signal about between each group, and the cross talk between groups can be decreased, on the whole, it can see and a cross talk can be decreased. Moreover, since the common internal electrode is prepared so that group correspondence may be countered synthetically, the passage cross section can be secured, and it can decrease loss, and can raise Q value as compared with the conventional example formed in individual internal electrode opposite in the shape of a ctenidium. Moreover, since between the community internal electrodes corresponding to a group is combined with a dielectric as compared with the structure where a common internal electrode is not divided, a strong big chip can be offered.

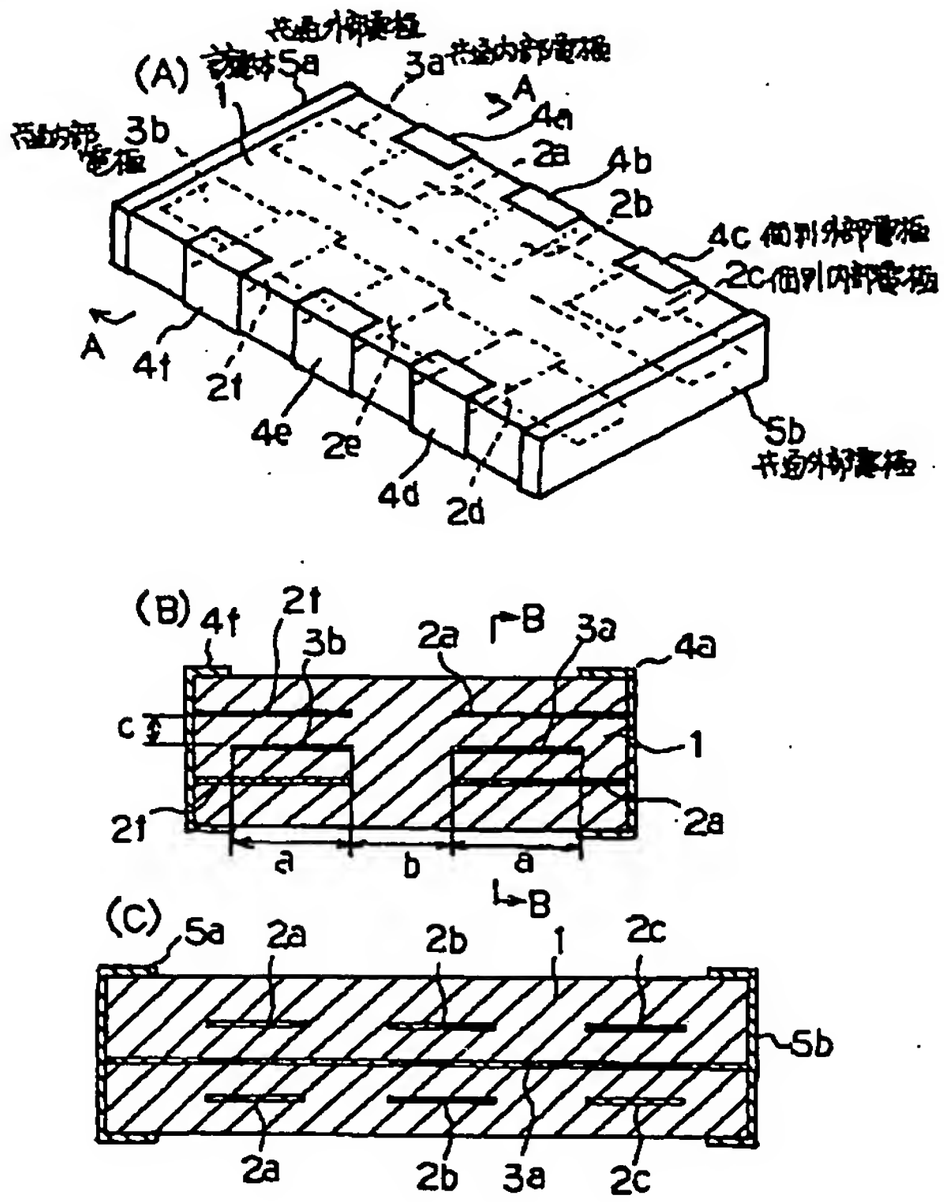
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]The A-A sectional view and (C of the perspective view showing one example of the capacitor array according [(A)] to this invention and (B)) are

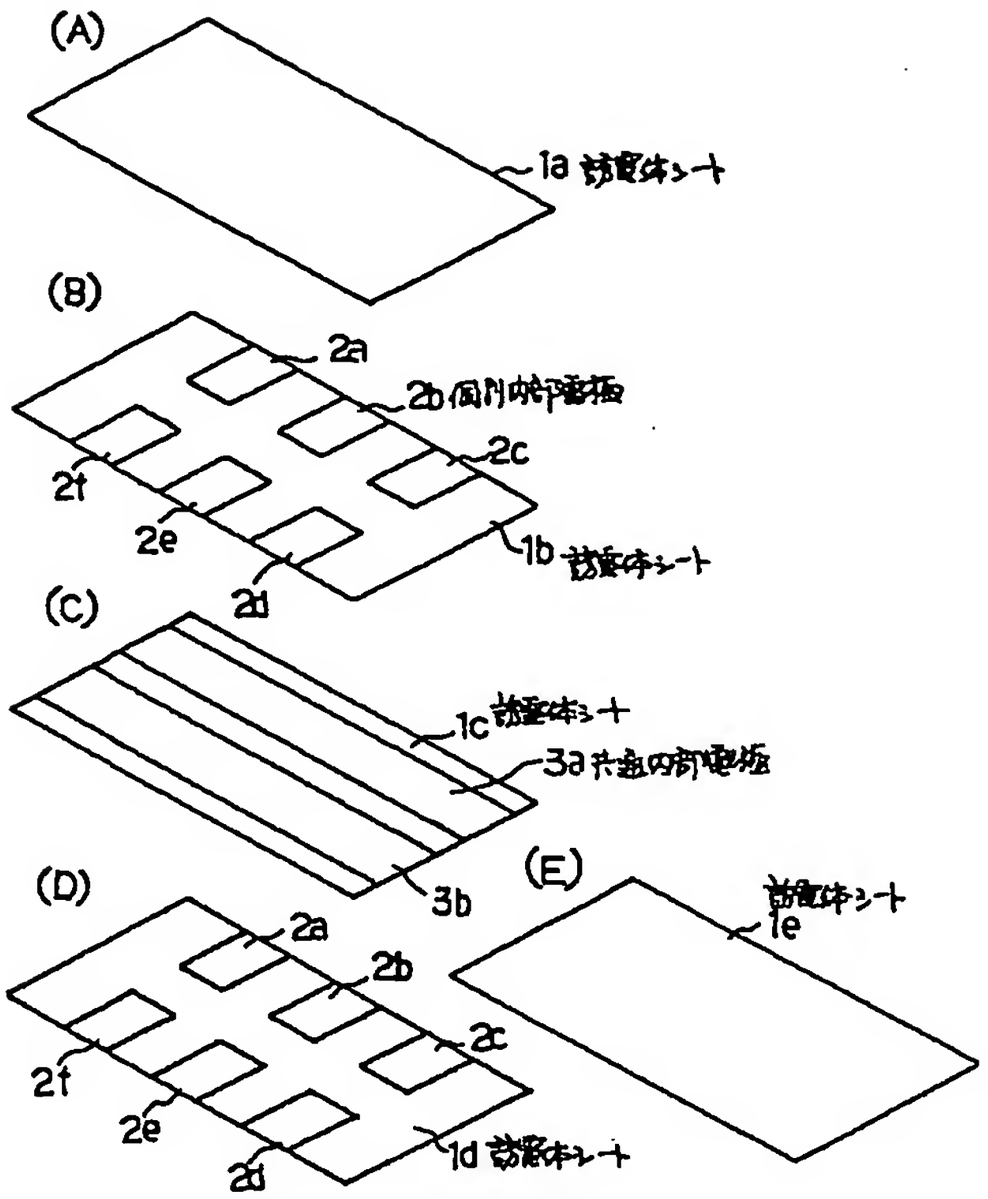
the B-B sectional views of (B).
[Drawing 2]It is drawing showing an example of the production process of this example.
[Drawing 3]It is drawing comparing and showing the cross talk property of this example and the conventional example.
[Drawing 4]The perspective view in which (A) shows the conventional capacitor array, and (B) are [the F-F sectional view of (B) and (D of the E-E sectional view and (C))] representative circuit schematics.
[Drawing 5]It is drawing showing the production process of the conventional example.
[Description of Notations]
1: A dielectric, a 2a-2f:individual internal electrode, 3a, a 3b:common internal electrode, a 4a-4f:individual external electrode, 5a, 5b : community external electrode

DRAWINGS

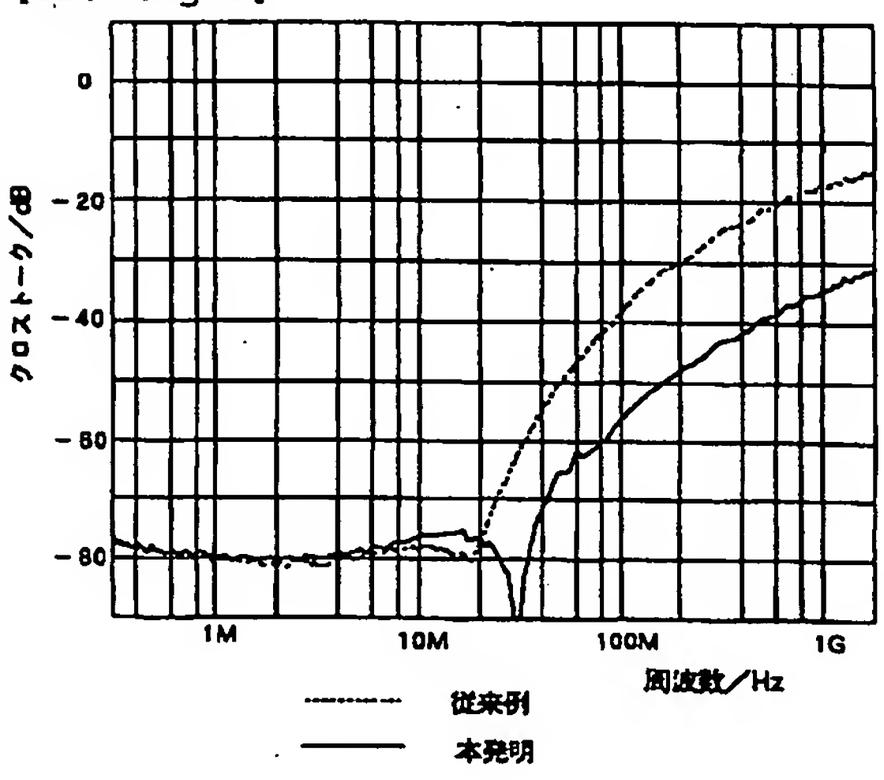
[Drawing 1]



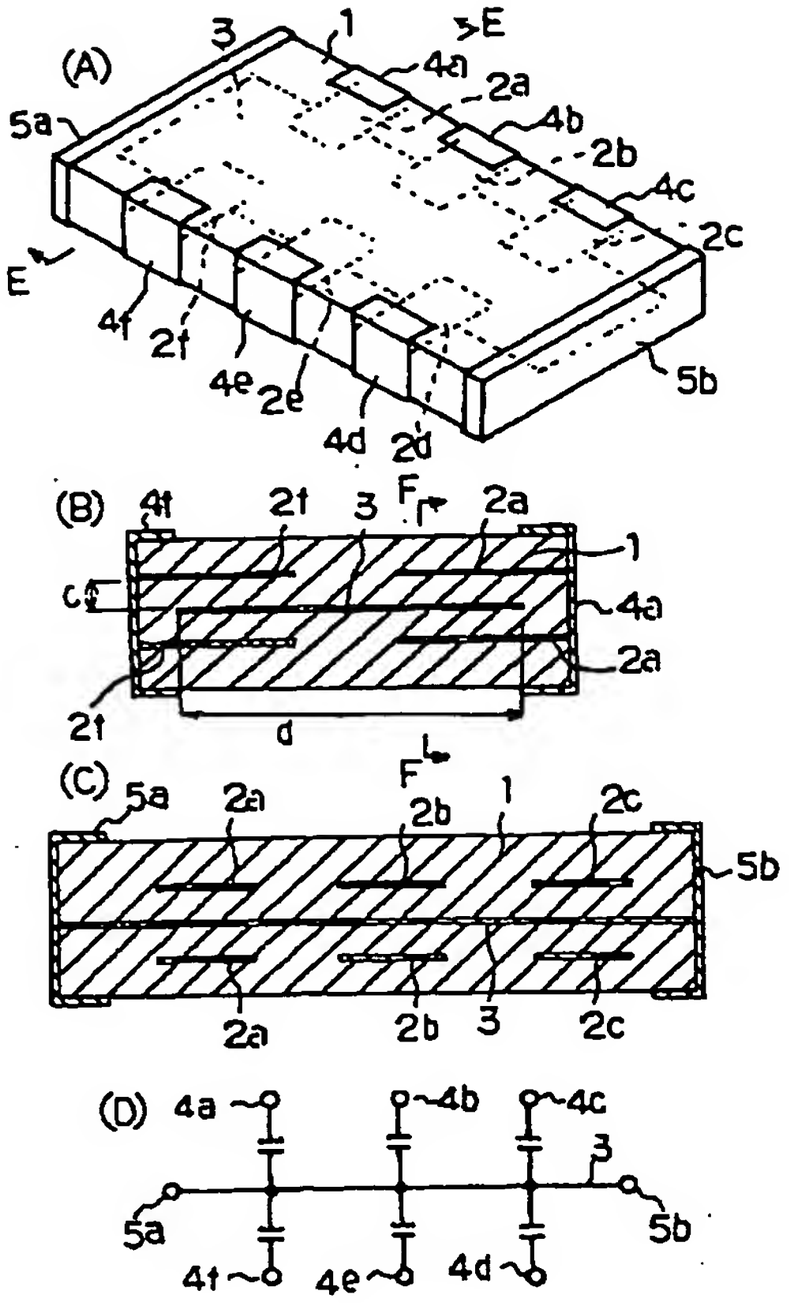
[Drawing 2]



[Drawing 3]



[Drawing 4]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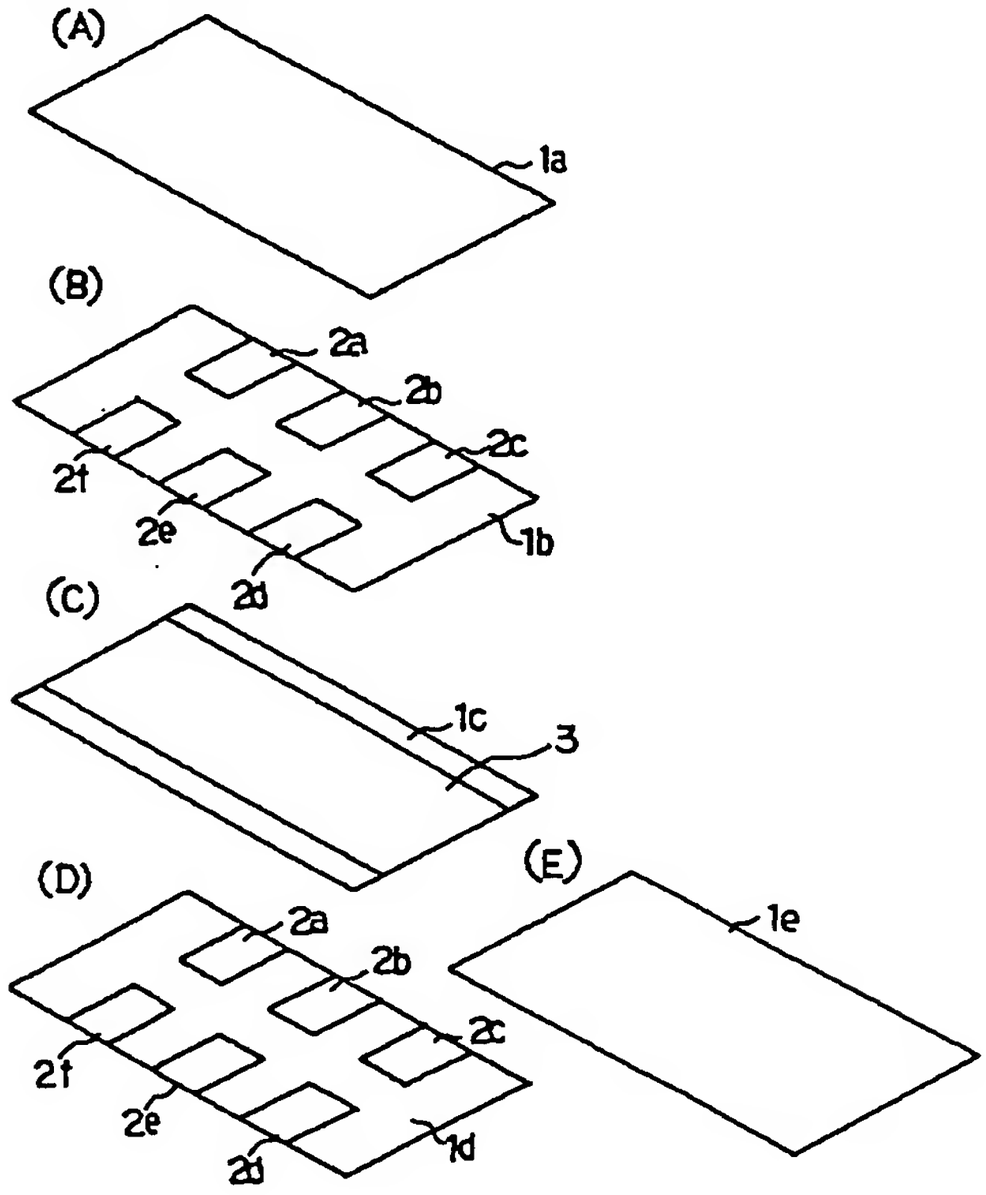
[Drawing 5]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